What is claimed is:

1. A one-bus multi-media computer system, comprising:

   a CPU/Sound/Graphic unit connected to a program and sound bus and a graphic bus;

   a bus arbitrator connected to said program and sound bus and said graphic bus on one side, and said one-bus on the other side;

   a program and sound and graphic memory connected to said one-bus; and

   a TV/LCD signal unit for outputting audio and video signals;

   said CPU/Sound/Graphic unit requests said program and sound and graphic memory by memory addresses, processes data returned from said program and sound and graphic memory, and sends the signals to said TV/LCD signal unit for outputting, said bus arbitrator sits between said CPU/Sound/Graphic and said program and sound and graphic memory to arbitrate said memory requests from said CPU/Sound/Graphic unit to said program and sound and graphic memory.

2. The system as claimed in claim 1, wherein said one-bus further comprises an address bus for sending address and a data bus for sending data.

3. The system as claimed in claim 1, wherein said program and sound bus further comprises an address bus for sending address and a data bus for sending data.

4. The system as claimed in claim 1, wherein said graphic bus further comprises an address bus for sending address and a data bus for sending data.

5. The system as claimed in claim 1, wherein said bus arbitrator uses the rule that a memory request to a faster memory is given a higher priority to access the bus without the pre-emptive capability.

6. The system as claimed in claim 5, wherein said bus arbitrator further comprises:

an address bus multiplexer having a first bus address and a second bus address as inputs, and an one-bus address as output, and

a first data register for storing data from one-bus, said one-bus data being controlled by a bus control signal called second bus signal OEB for temporarily stored in said first data register or directly outputted to a second data bus.

7. The system as claimed in claim 6, wherein said first bus is a low frequency program and sound system bus, and said second bus is a high frequency video bus.

8. The system as claimed in claim 6, wherein said second bus signal OEB controls the operation of said address multiplexer and said first data register with the following rules:

(a) when said second bus signal OEB is low, said address bus multiplexer takes said second bus address and outputs one-bus address, at the same time, said first data bus register stores said one-bus data and outputs said first bus data;

(b) when said second bus signal OEB is high, it is the accessing cycle for said first bus untill said second bus signal OEB becomes low, during the accessing cycle of said first bus, one-bus data is transported to said first bus data; and

(c) said second bus gets said second bus data before said second bus signal OEB transits from low to high.

9. A system chip for processing audio and video data, comprising:

a CPU/Sound/Graphic unit connected to a program and sound bus and a graphic bus;

a bus arbitrator connected to said program and sound bus and said graphic bus on one side, and a one-bus on the other side;

a program and sound and graphic memory connected to said one-bus; and

a TV/LCD signal unit for outputting audio and video signals;

said CPU/Sound/Graphic unit requests said program and sound and graphic memory by memory addresses, processes data returned from said program and sound and graphic memory, and sends the signals to said TV/LCD signal unit for outputting, said bus arbitrator sits between said CPU/Sound/Graphic and said program and sound and graphic to arbitrate said memory requests from said CPU/Sound/Graphic unit to said program and sound and graphic memory.